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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,316	BERNDLMAIER ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed February 24, 2004 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-4, 6, 8-11, 13, 15-18, 20, 22-25, & 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Childers et al. US Pat no. 6,877,117 B1.

As per claim 1:

Childers et al. teaches a self-monitoring (Figure 2 # 16) and self-correcting (Figure 2 # 30) integrated circuit device comprising: a self-testing controller (Figure 2 # 22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device; a comparator adapted

to evaluate whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

As per claim 2:

Childers et al. teaches the integrated circuit, wherein said performance self-testing comprises one or more of a built-in self test (BIST) unit (Figure 2 # 20, column 2, lines 25-28) and a functional testing unit (column 5, lines 50-55).

As per claim 3:

Childers et al. teaches the integrated circuit, wherein said functional testing unit is adapted to apply functional test sequences (column 5, lines 50-55) to said integrated circuit device until failure (column 5, lines 40-48), and said comparator compares the failure frequency against predetermined limits (column 5, lines 22-27).

As per claim 4:

Childers et al. teaches the integrated circuit, wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit device (column 6, lines 21-25).

As per claim 6:

Childers et al. teaches the integrated circuit wherein said processor adjusts said parameters by permanently altering the voltage produced by voltage regulators (column 6, lines 21-25).

As per claim 8:

Childers et al. teaches an autonomously self-monitoring (Figure 2 # 16) and self-correcting (Figure 2 # 30) integrated circuit device comprising: a self-testing controller adapted to periodically perform performance self-testing (Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device throughout the useful life of said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and a processor adapted to permanently self-adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

As per claim 9:

Childers et al. teaches the integrated circuit, wherein said performance self-testing comprises one or more of a built-in self test (BIST) unit (Figure 2 # 20, column 2, lines 25-28) and a functional testing unit (column 5, lines 50-55).

As per claim 10:

Childers et al. teaches the integrated circuit, wherein said functional testing unit is adapted to apply functional test sequences (column 5, lines 50-55) to said integrated circuit device until failure (column 5, lines 40-48), and said comparator compares the failure frequency against predetermined limits (column 5, lines 22-27).

As per claim 11:

Childers et al. teaches the integrated circuit, wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit device (column 6, lines 21-25).

As per claim 13:

Childers et al. teaches the integrated circuit, wherein said processor adjusts said parameters by permanently altering the voltage produced by voltage regulators (column 6, lines 21-25).

As per claim 15:

Childers et al. teaches a method of continuously monitoring (Figure 2 # 16) and adjusting (Figure 2 # 30) the operation of an integrated circuit device, said method comprising: periodically performing performance testing Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device; evaluating whether results from said testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and adjusting parameters of said integrated circuit device until said results from said testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

As per claim 16:

Childers et al. teaches the method, wherein said performance testing comprises one of built-in self testing (BIST) (Figure 2 # 20, column 2, lines 25-28) and functional tests (column 5, lines 50-55).

As per claim 17:

Childers et al. teaches the method, wherein said functional tests comprise looping (column 5, lines 50-55) through functional test sequences until failure (column 5, lines 40-48), and said evaluating of said results compares the failure frequency against predetermined limits (column 5, lines 22-27).

As per claim 18:

Childers et al. teaches the method, wherein said process of adjusting said parameters comprises altering the voltage supplied to portions of said integrated circuit device (column 6, lines 21-25).

As per claim 20:

Childers et al. teaches 20 the method, wherein said process of adjusting said parameters comprises permanently altering the voltage produced by voltage regulators (column 6, lines 21-25).

As per claim 22:

Childers et al. teaches a method of autonomously self-monitoring (Figure 2 # 16) and self-adjusting (Figure 2 # 30) the operation of an integrated circuit device throughout the useful life of said integrated circuit device, said method comprising: periodically performing performance self-testing (Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device throughout the integrated circuit devices useful life; evaluating whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and self-adjusting parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

As per claim 23:

Childers et al. teaches the method, wherein said performance self-testing comprises one of built-in self testing (BIST) (Figure 2 # 20, column 2, lines 25-28) and functional tests (column 5, lines 50-55).

As per claim 24:

Childers et al. teaches the method, wherein said functional tests comprise looping (column 5, lines 50-55) through functional test sequences until failure (column 5, lines 40-48), and said evaluating of said results compares the failure frequency against predetermined limits (column 5, lines 22-27).

As per claim 25:

Childers et al. teaches the method, wherein said process of self-adjusting said parameters comprises altering the voltage supplied to portions of said integrated circuit device (column 6, lines 21-25).

As per claim 27:

Childers et al. teaches the method, wherein said process of self-adjusting said parameters comprises permanently altering the voltage produced by voltage regulators (column 6, lines 21-25).

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 5, 12, 19 & 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Childers et al. US Pat no. 6,877,117 B1, and further in view of Bartlett et al. US Pat no. 3,761,882.

As per claim 5:

Childers et al. substantially teaches a self-monitoring (Figure 2 # 16) and self-correcting (Figure 2 # 30) integrated circuit device comprising: a self-testing controller (Figure 2 # 22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the integrated circuit, further comprising electronic fuses, wherein said processor is adapted to activate said electronic fuses to permanently change said parameters of said integrated circuit device.

However, Bartlett et al. in an analogous art teaches the integrated circuit, further comprising electronic fuses (column 19, lines 1-3) wherein said processor is adapted to activate said electronic fuses to permanently change said parameters of said integrated circuit device (column 19, lines 4-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert fuses near the microprocessor circuit or the potentiometer to enable Childers invention to permanently change voltage or to protect a certain circuit element in the case of variable voltage.

As per claim 12:

Childers et al. substantially teaches an autonomously self-monitoring (Figure 2 # 16) and self-correcting (Figure 2 # 30) integrated circuit device comprising: a self-testing controller adapted to periodically perform performance self-testing (Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device throughout the useful life of said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and a processor adapted to permanently self-adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the integrated circuit, further comprising electronic fuses, wherein said processor is adapted to activate said electronic fuses to permanently change said parameters of said integrated circuit device.

However, Bartlett et al. in an analogous art teaches the integrated circuit, further comprising electronic fuses (column 19, lines 1-3) wherein said processor is adapted to activate said electronic fuses to permanently change said parameters of said integrated circuit device (column 19, lines 4-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert fuses near the microprocessor circuit or the potentiometer to enable Childers invention to permanently change voltage or to protect a certain circuit element in the case of variable voltage.

As per claim 19:

Childers et al. substantially teaches a method of continuously monitoring (Figure 2 # 16) and adjusting (Figure 2 # 30) the operation of an integrated circuit device, said method comprising: periodically performing performance testing Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device; evaluating whether results from said testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and adjusting parameters of said integrated circuit device until said results from said testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the method, wherein said process of adjusting said parameters comprises activating electronic fuses to permanently change said parameters of said integrated circuit device.

However, Bartlett et al. in an analogous art teaches a method, wherein said process of adjusting said parameters comprises activating electronic fuses (column 19, lines 1-3) to permanently change said parameters of said integrated circuit device (column 19, lines 4-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert fuses near the microprocessor circuit or the potentiometer to enable Childers invention to permanently change voltage or to protect a certain circuit element in the case of variable voltage.

As per claim 26:

Childers et al. substantially teaches a method of autonomously self-monitoring (Figure 2 # 16) and self-adjusting (Figure 2 # 30) the operation of an integrated circuit device throughout the useful life of said integrated circuit

device, said method comprising: periodically performing performance self-testing (Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device throughout the integrated circuit devices useful life; evaluating whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and self-adjusting parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the method, wherein said process of self-adjusting said parameters comprises activating electronic fuses to permanently change said parameters of said integrated circuit device.

However, Bartlett et al. in an analogous art teaches a method, wherein said process of self-adjusting said parameters comprises activating electronic fuses (column 19, lines 1-3) to permanently change said parameters of said integrated circuit device (column 19, lines 4-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert fuses near the microprocessor circuit or the potentiometer to enable Childers invention to permanently change voltage or to protect a certain circuit element in the case of variable voltage.

Claims 7, 14, 21 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Childers et al. US Pat no. 6,877,117 B1, and further in view of Porter et al. US Pat no. 5,263,032.

As per claim 7:

Childers et al. substantially teaches a self-monitoring (Figure 2 # 16) and self-correcting (Figure 2 # 30) integrated circuit device comprising: a self-testing controller (Figure 2 # 22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the integrated circuit further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor.

However, Porter et al. in an analogous art teaches the integrated circuit further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor (column 6, lines 51-68). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a storage device to record the error information being outputted on line 36 (Figure 2) by the Error Detection & Correction Circuit (column 5, lines 42-48). It would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have realized that storing the error information in an error log would allow for a better analysis of the parentage error. Further the use of error logs and storing error information is commonly know in the art and is used in various inventions, which employ various circuit testing techniques.

As per claim 14:

Childers et al. substantially teaches an autonomously self-monitoring (Figure 2 # 16) and self-correcting (Figure 2 # 30) integrated circuit device comprising: a self-testing controller adapted to periodically perform performance self-testing (Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device throughout the useful life of said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and a processor adapted to permanently self-adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the integrated circuit further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor.

However, Porter et al. in an analogous art teaches the integrated circuit further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor (column 6, lines 51-68). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a storage device to record the error information being outputted on line 36 (Figure 2) by the Error Detection & Correction Circuit (column 5, lines 42-48). It would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have realized that storing the error information in an error log would allow for a better analysis of the parentage

error. Further the use of error logs and storing error information is commonly know in the art and is used in various inventions, which employ various circuit testing techniques.

As per claim 21:

Childers et al. teaches a method of continuously monitoring (Figure 2 # 16) and adjusting (Figure 2 # 30) the operation of an integrated circuit device, said method comprising: periodically performing performance testing Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device; evaluating whether results from said testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and adjusting parameters of said integrated circuit device until said results from said testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the method, further comprising maintaining a history of adjustments made to said parameters during said adjusting process.

However, Porter et al. in an analogous art teaches the method, further comprising maintaining a history of adjustments made to said parameters during said adjusting process (column 6, lines 51-68). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a storage device to record the error information being outputted on line 36 (Figure 2) by the Error Detection & Correction Circuit (column 5, lines 42-48). It would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have realized that storing the error information in an

error log would allow for a better analysis of the parentage error. Further the use of error logs and storing error information is commonly know in the art and is used in various inventions, which employ various circuit testing techniques.

As per claim 28:

Childers et al. substantially teaches a method of autonomously self-monitoring (Figure 2 # 16) and self-adjusting (Figure 2 # 30) the operation of an integrated circuit device throughout the useful life of said integrated circuit device, said method comprising: periodically performing performance self-testing (Figure 2 # 22, column 5, lines 15-21) on said integrated circuit device throughout the integrated circuit devices useful life; evaluating whether results from said self-testing are within acceptable limits (Figure 2 # 16, column 5, lines 21-28); and self-adjusting parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (Figure 2 # 42, column 5, lines 16-25).

Childers et al. does not explicitly teach the method, further comprising maintaining a history of adjustments made to said parameters during said self-adjusting process.

However, Porter et al. in an analogous art teaches the method, further comprising maintaining a history of adjustments made to said parameters during said self-adjusting process (column 6, lines 51-68). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to insert a storage device to record the error information being outputted on line 36 (Figure 2) by the Error Detection & Correction Circuit (column 5, lines 42-48). It

would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have realized that storing the error information in an error log would allow for a better analysis of the parentage error. Further the use of error logs and storing error information is commonly know in the art and is used in various inventions, which employ various circuit testing techniques.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 6487352 B1, US Pat no. 5325397 A, US Pat no. 6115157 A, US Pat no. 6307899 B1, US Pat no. 5263032 A, and US PG-Pub no. 20020056063 A1 mention the same self-testing procedure which constitutes self-monitoring and self-adjusting the circuit parameters are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
02/08/2006

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